Notice of Allowability	Application No.	Applicant(s)	
	10/614,961	MANDELMAN ET AL.	
	Examiner	Art Unit	
	Jennifer M. Kennedy	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the preliminary amendment filed 7/8/2003*.

2. ☒ The allowed claim(s) is/are *13-21*.

3. ☒ The drawings filed on *25 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/8/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jay H. Anderson on April 15, 2004.

The application has been amended as follows:

In claim 19, after line 13, and before line 14, insert

--a contact area on said bottom surface of said device layer outside said trenches;--

In claim 19, line 17, the second instance of "buried" should be replaced with –bottom--.

The following is an examiner's statement of reasons for allowance: the prior art, either singly or in combination, fails to anticipate or render obvious, method, including the limitations an integrated circuit having a device layer of semiconductor with a device layer thickness of less than 100nm above an array insulating layer and containing an array of DRAM cells including a trench capacitor connected by a buried strap to a horizontal pass transistor formed in said device layer, said pass transistor having an

internal contact adjacent said trench, in which said buried strap is formed from strap conductive material extending vertically in said trenches to a level below said bottom surface of said device layer and laterally outside said trenches and underneath said internal contact of said pass transistor, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps in combination with the other limitations of independent claim 13.

Further, the prior art, either singly or in combination, fails to anticipate or render obvious, method, including the limitations of an integrated circuit having a device layer of semiconductor with a device layer thickness of less than 100 nm above an array insulating layer and containing an array of DRAM cells disposed in a first subset of DRAM cells and a second subset of DRAM cells, including a trench capacitor formed at an edge of said DRAM cells and connected by a buried strap to a horizontal pass transistor formed in said device layer and displaced laterally from said trench capacitor, comprising a contact area on said bottom surface of said device layer outside said trenches, strap conductive material disposed in said trenches to a level above said bottom surface of said device layer, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps, a set of horizontal cell pass transistors in said device layer having cell electrodes, transistor gates disposed above said device layer and connected to a first subset of interconnect lines and internal electrodes in contact with said buried traps through said contact area and separated from an adjacent trench by said isolating trenches in combination in with the other limitations of independent claim 16.

Further, the prior art, either singly or in combination, fails to anticipate or render obvious, method, including the limitations of an integrated circuit having a device layer of semiconductor with a device layer thickness of less than 100 nm above an array insulating layer and containing an array of DRAM cells disposed in a first subset of DRAM cells and a second subset of DRAM cells, including a trench capacitor formed at an edge of said DRAM cells and connected by a buried strap to a horizontal pass transistor formed in said device layer and displaced laterally from said trench capacitor, comprising a contact area on said bottom surface of said device layer outside said trenches, a conformal liner of conductive material disposed in said trenches to a level above said bottom surface of said device layer, whereby said liner of conductive material makes electrical contact with a bottom surface of said device layer at the location where said buried strap meets said bottom surface, strap conductive material disposed in said trenches to a level above said bottom surface of said device layer, whereby said strap conductive material makes electrical contact with said bottom surface to form said buried straps, a set of horizontal cell pass transistors in said device layer having cell electrodes, transistor gates disposed above said device layer and connected to a first subset of interconnect lines and internal electrodes in contact with said buried strap through said contact area and separated from an adjacent trench by said isolating trenches in combination with the other limitations of independent claim 19.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Drawings

The drawings were received on March 25, 2204. These drawings are acceptable.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Kennedy whose telephone number is (571) 272-1672. The examiner can normally be reached on Mon.-Fri. 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmk

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